

Amendment and Response under 37 C.F.R. 1.116

Applicant: Thomas C. Anthony
Serial No.: 10/612,676
Filed: July 2, 2003
Docket No.: 10014296-1
Title: MAGNETIC MEMORY DEVICE

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims:

1. (Currently Amended) A memory wafer comprising:
a first surface having a plurality of unseparated memory chips disposed thereon, the memory chips defining an exterior face of the memory wafer;
a second surface opposite the exterior face; and
a magnetically permeable shield layer extending over the entirety of at least one of the exterior face and the second surface of the memory wafer.
2. (Original) The memory wafer of claim 1, wherein the memory chips are separable from the memory wafer.
3. (Original) The memory wafer of claim 1, wherein the memory chips are magnetic random access memory chips.
4. (Original) The memory wafer of claim 1, wherein the memory chips include multiple memory arrays having multiple memory cells.
5. (Original) The memory wafer of claim 4, wherein the memory cells are magnetic random access memory cells.
6. (Original) The memory wafer of claim 1, further comprising bond pads disposed on the memory chips.
7. (Original) The memory wafer of claim 6, wherein the bond pads are electrically accessible via the exterior face of the memory wafer.

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8. (Original) The memory wafer of claim 1, wherein the magnetically permeable shield layer comprises a soft magnetic material.

9. (Original) The memory wafer of claim 8, wherein the soft magnetic material is selected from the group consisting of iron, nickel, cobalt, alloys of iron, alloys of nickel, and alloys of cobalt.

10. (Original) The memory wafer of claim 1, wherein the magnetically permeable shield layer has a permeability of greater than 100.

11. (Original) The memory wafer of claim 1, wherein the magnetically permeable shield layer has a coercivity of less than 10 Oersteds.

12. (Original) The memory wafer of claim 1, wherein the magnetically permeable shield layer is isotropic.

13-17. (Cancelled)

18. (Withdrawn) A method of shielding a memory device from stray magnetic fields, the method comprising:

providing a memory wafer having a plurality of separable memory chips defining an exterior face and a second surface opposite the exterior face; and

attaching a magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer.

19. (Withdrawn) The method of claim 18, further comprising electrically accessing bond pads disposed on the separable memory chips by a process selected from the group consisting of photolithographic patterning/etching, chemical mechanical planarization, mechanical abrasion, and chemical etching.

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20. (Withdrawn) The method of claim 18, wherein attaching the magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer comprises a process selected from the group consisting of sputtering, evaporation, electroplating, electroless plating and chemical vapor deposition.

21. (Withdrawn) The method of claim 18, wherein attaching the magnetically permeable shield layer includes attaching the magnetically permeable shield layer in the presence of a magnetic field.

22. (Withdrawn) The method of claim 21, wherein attaching the magnetically permeable shield layer in the presence of the magnetic field includes rotating the magnetic field.

23. (Withdrawn) The method of claim 18, wherein attaching the magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer comprises:

depositing the magnetically permeable shield layer; and

annealing the magnetically permeable shield layer in a magnetic field.

24. (Withdrawn) The method of claim 23, wherein annealing the magnetically permeable shield layer in a magnetic field includes annealing the magnetically permeable shield layer in a rotating magnetic field.

25. (Withdrawn) The method of claim 18, wherein attaching the magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer comprises depositing the magnetically permeable shield layer onto a rotating memory wafer in the presence of a stationary magnetic field.

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26. (Withdrawn) The method of claim 18, wherein attaching the magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer comprises depositing the magnetically permeable shield layer in a rotating magnetic field.

27. (Withdrawn) The method of claim 23, wherein annealing the magnetically permeable shield layer includes annealing the magnetically permeable shield layer at a temperature that is lower than an annealing temperature of a magnetic material in the memory wafer.

28. (Withdrawn) The method of claim 25, wherein depositing the magnetically permeable shield layer onto the rotating memory wafer in the presence of the stationary magnetic field forms an isotropic magnetically permeable shield layer.

29. (Currently Amended) A memory wafer comprising:
a first surface having a plurality of unseparated memory chips disposed thereon, the memory chips defining an exterior face of the memory wafer;
a second surface opposite the exterior face; and
means for protecting the memory ~~cells-chips~~ from stray magnetic fields
extending over the entirety of at least one of the exterior face and the second
surface of the memory wafer.

30. (Currently Amended) The memory wafer of claim 29, wherein the means for protecting the memory ~~cells-chips~~ from stray magnetic fields is a magnetically permeable shield layer comprising a soft magnetic material.

31. (Original) The memory wafer of claim 30, wherein the magnetically permeable shield layer has a permeability of greater than 100.

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32. (Original) The memory wafer of claim 30, wherein the magnetically permeable shield layer has a coercivity of less than 10 Oersteds.

33. (Cancelled)